MULTILEVEL INVERTER AND ITS LIMITATIONS WHEN APPLIED AS STATCOM

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Abstract---**This paper deal with multilevel inverter applied as STATCOM and its limitations. We show that "of line" optimization of switching angles used together with fundamental frequency modulation switching strategy (FFM) does not allow proper compensation during unbalanced condition. Instead, pulse with modulation switching strategy (PWM) must be used during unbalanced operation of the system.**

Index Terms---- **STATCOM, multilevel voltage source inverter, unbalanced condition, fundamental frequency modulation switching strategy.**

I. INTRODUCTION

REACTIVE power compensation is one of the most important action for control of power systems on transmission and distribution level. It allows better stability of overall system, decrease losses and permit to maintain better voltage profile. The compensated power system is less prone to failure than a non compensated one. For last ten years there have been a tendency to replace the traditional compensators with FACTS devices that are based on power converters. The shunt capacitors and inductances can be replaced with STATCOM and series capacitors with SSSC (Series Static Synchronies Compensator). These devices have advantages of fast response and they need a considerably smaller amount of real estate for their installation. Their main drawbacks are switching and conduction losses. Moreover, voltage rating of switching devices is not high enough. The switches of choice for high voltage applications are GTOs and their voltage rating is about 6000 V till now. To increase the voltage rating of the power converter and so of the overall FACTS controllers, different multilevel topologies have been proposed [1]. One of the multilevel topologies that draw a lot of attention is so called diode clamped voltage source inverter. For the purpose of our study we fabricated one five level diode clamped voltage source inverter (VSI). The inverter is applied as STATCOM.

The main advantages of diode clamped VSI when applied as STATCOM over its six pulses counterpart is in fact that by increasing number of levels the voltage rating of inverter is increased and at the same time the total harmonic distortion (THD) of the inverter output voltage is decreased while fundamental frequency modulation (FFM) switching strategy is used. As switching devices we used IGBTs. The inverter circuit is controlled by one DSP box. In spate of its good performance when applied in reactive power compensation of balanced load we noticed that is impossible to compensate for unbalanced load if FFM switching strategy is applied together with off line optimization. In this paper we discuss limitations of multilevel diode clamped VSI when applied in reactive power compensation of unbalanced load. The simulation and experimental results are presented and solution proposed.

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II. DIODE CLAMPED VOLTAGE SOURCE INVERTER

The topology was proposed in [2] had initially only three levels and has been controlled by PWM modulation strategy. The three levels diode clamped VSI gained a lot of attention for high voltage application and very soon has been upgraded with the new levels [3-4] and enhanced [5-6]. Because of its advantages as decreased THD, off-line optimization of switching angles, increased voltage rating and diminished dv/dt stress, the topology has been suggested for different high voltage application as STATCOM, UPFC and back to back DC link. However, there are some important drawbacks as complicated construction and capacitors voltage balancing problem. The capacitor voltage unbalance depends upon switching angles and net active power transferred between AC and DC side of inverter. If this transfer is zero than the problem disappears. Because of capacitor voltage balancing problem, the suitable applications for diode clamped multilevel VSI is as STATCOM. In the case of ideal STATCOM the net active power exchange between AC and DC side of inverter circuit is zero during steady state operation.

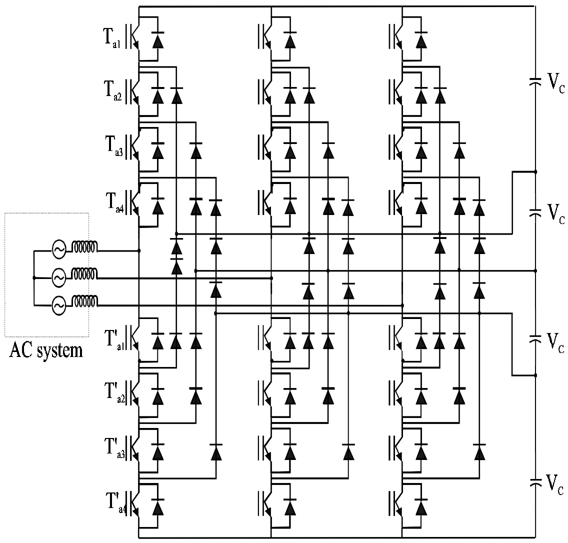

Fig.1. Power circuit of five level diode clamped VSI

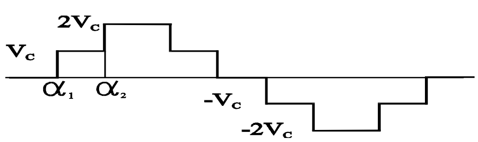

Fig.2. Five level inverter output voltage waveform

Fig.1 shows a three-phase five level diode clamped VSI. The DC bus consists of four capacitors that allow five taps for five levels of voltage. One phase of five level inverter consist of eight power switches (IGBTs in our case) and six clamping diodes. Each IGBT has one diode connected in anti-parallel so that is bi-directional in current and uni-directional in voltage. The one phase of inverter is capable of constructing five level staircase output voltage (fig.2) while FFM switching strategy is applied. The line to line voltage can be seven or nine level, depending on switching angles α_1 and α_2.

III. Fundamental Frequency Modulation Switching Strategy

Fundamental frequency modulation (FFM) switching strategy is conceived on premise that each switch commute only twice over one cycle of fundamental frequency (once on and once off). This strategy of modulation may be difficult to accept in case of six pules inverter because of large amount of pollution in output voltage waveform, but in case of multilevel inverter, if number of level is sufficiently high the distortion presented in output voltage is small enough. Moreover, FFM is crucial for high voltage application because it allows considerable decrease of switching losses. Fig.3 shows switching functions that allows generation of stair case output voltage shown in fig.2. The hashed areas means that switch is gated.

- For voltage level $2V_C$ all upper switches T_1through T_4 are on
- For voltage level V_C switches T_2,T_3 and T_4 are on, T_1 is off
- For voltage level 0 switches T_3 and T_4 are on, T_1 and T_2 are off
- For voltage level $-V_C$ switches T_4 is on, T_1,T_2,T_3 are off
- For voltage level $-2V_C$ all upper switches are off

The switches T'_1through T'_4 are complimentary with switches T_1through T_4 .

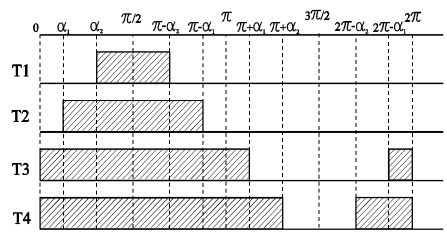

Fig.3. Switching function

The inverter phase output voltage (Fig.2) can be represented by Fourier series :

$$v(t)=\sum_{k=1}^{\infty}\frac{4V_C}{\pi k}\left[\cos k\alpha_1+\cos k\alpha_2\cdots\cos k\alpha_{\frac{N-1}{2}}\right]\sin k\omega t \quad k=2n+1,\quad n\in N \qquad (1)$$

N-number of the levels

In our case N=5 so the amplitude of fundamental component is:

$$v_1(t)=\frac{4V_C}{\pi}\left[\cos\alpha_1+\cos\alpha_2\right] \qquad (2)$$

and rms value is(3):

$$V_{1rms}^2=\frac{8V_C^2}{\pi^2}\left[\cos\alpha_1+\cos\alpha_2\right]^2 \qquad (3)$$

The switching angles α_1 and α_2 are chosen to cancel 5^{th} end 7^{th} harmonics. The 3^{rd} and its multiples will cancel itself in three phase balanced system. From (2) and (3) it is obvious that magnitude and rms value of fundamental component of inverter output voltage depends on switching angles α_1 and α_2, and on dc bus voltage. When angles are off line chosen, than value of (2) and (3) depend exclusively on dc bus voltages Vc.

IV. Fundamentals Of STATCOM

Static compensators based on inverter circuit (STATCOM) are mostly designed for voltage support of three-phase balanced systems. On transmission level, systems are normally balanced, but it is not a case during the fault conditions or in distribution system. In three phase balanced system STATCOM produce a set of balanced reactive currents so that instantaneous power flow in STATCOM or from STATCOM is always zero. It means that, at each moment, instantaneous power brought to the STATCOM by one phase is equal to the instantaneous power taken away from the STATCOM by other two phases and vice versa. The zero instantaneous power flow permits the use of small capacitors on the DC side of inverter. The role of those capacitors is to keep DC voltage on a suitable level that satisfies reactive needs of the load and not to store large amount of energy. Physically, compensator based on a three phase inverter circuit interconnects all three phases of three phase AC system, providing path for exchange of reactive power between them [7,8]. This type of exchange is disturbed during unbalance operation of the AC system. In this case each phase of inverter must provide unequal voltage. If PWM strategy of control is used, it is possible to change phase voltages by changing control signals and keeping DC voltage constant[9]. The value of DC reference voltage will determine the rating of the inverter and the inverter will always draw some active power from AC system to cover for its losses and to keep the DC bus voltage constant. If hysteresis current control is applied, harmonics can be compensated and the inverter will act as an active filter [10]. But both command strategies mentioned above impose high switching frequency and hence high switching losses. To avoid high switching losses, fundamental frequency modulation strategy (FFM) for control of multilevel inverter has been suggested [11]-[13]where the control of reactive power is achieved by controlling power angle which permits charging and discharging of DC side capacitors of inverter resulting in the control of the fundamental component of inverter output voltage. When more reactive power is needed, the inverter output voltage is made to lag the phase voltage of the AC system allowing power to flow from the AC system into the inverter, boosting voltage in its DC bus capacitors. With boost in DC bus voltage, output voltage waveform of all three phases of inverter are affected. To get three unequal output voltages, one solution is to shift switching angles (there are many switching angles because commercially applied STATCOM must be made of many six pulses inverter or some other multilevel topology are to be used), but it means online computation and introduction of additional distortion in to the system. Moreover, shifting switching angels will introduced distortion that is variable so it can be difficult to clear.

V. Simulation And Experimental Results

The multilevel inverter is applied for power factor correction of a R-L load. The control algorithm is given in [14,15]. As simulation tools we used “Power System Blockset” and “Simulink” The switching angles are off line chosen in order to cancel 5th and 7th harmonic. Their values are 5.134° and 30.857°. The harmonic spectra of phase voltage is shown in fig.4 and line to line voltage in fig.5 From harmonic spectra of phase voltage it can be clearly seen that 5th and 7th harmonics are canceled. The THD obtained in phase voltage is 21.7% (fig.4). In line to line voltage 3rd harmonic in its multiples are eliminated and the THD is only 8.56% (fig.5).

Fig.6 shows DC response and fig.7 AC response of all three phases of the STATCOM. The increase in AC voltage produced by inverter is consequence of voltage boost in DC bus. The all three inverter phase currents are leading the inverter voltage for 90 degrees. It is obvious that boost in DC bus voltage affects equally all three inverter output voltage. Fig.8 shows results of compensation. Fig.8-a shows voltage and current supplied by the source before compensation, fig.8-b shows inverter output voltage and current and fig.8-c shows voltage supplied by the source and current of the load and the current of the source after compensation. It is clear that current supplied by the source is decreased and returned in the phase with voltage supplied by the source.

To confirm simulation results, a prototype of diode clamped VSI using IGBTs as switching devices is constructed. For control circuit, a DSP box is used and AC output voltage is phase locked with source voltage. Fig.9 shows the inverter output voltage with its harmonic spectra. Fig.10 shows line voltage that consist of nine level. Fig. 11 shows one phase of the source voltage and the current before compensation (upper trace) and the inverter voltage and current (lower trace). It can be clearly seen that current supplied by the source is inductive. The load used for the experiment is unbalanced. Fig. 12 shows the source voltage and the current (upper trace) and inverter voltage and currant (lower trace) after compensation. The current supplied by the source is returned in phase with the voltage and decreased by 60%. The power factor is corrected from 0.2 to 0.98. The compensator current (lower trace) is capacitive and STATCOM does not absorb any net active power. There is large amount of third harmonic present an it does not cancel because of unbalanced condition. Moreover, just one phase can be properly compensated.

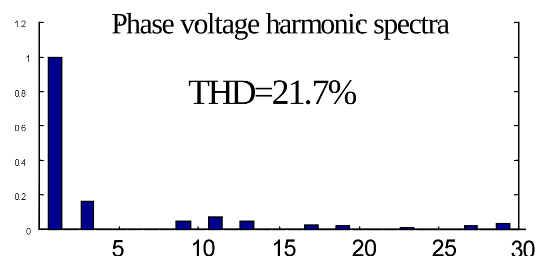

Fig.4. The harmonic spectra of phase voltage

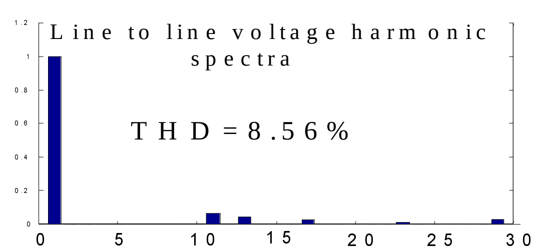

Fig. 5. The harmonic spectra of line voltage

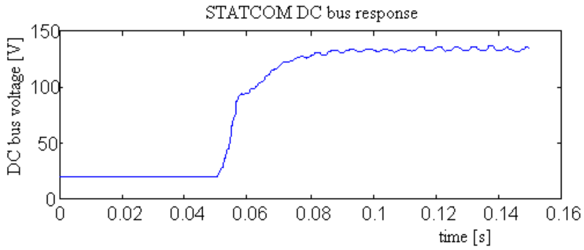

Fig.6. STATCOM DC response

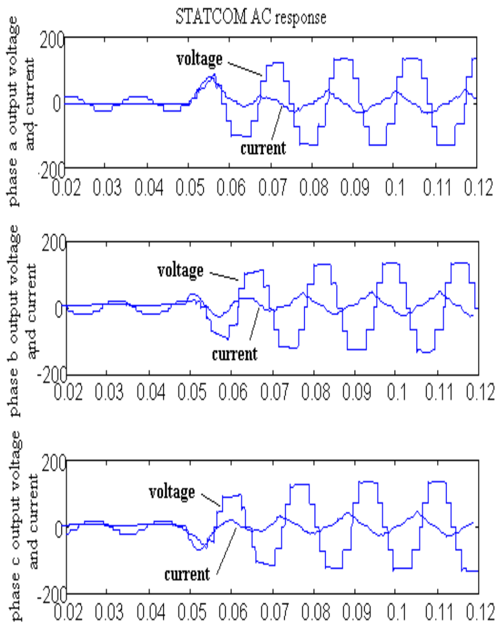

Fig.7. STATCOM AC response

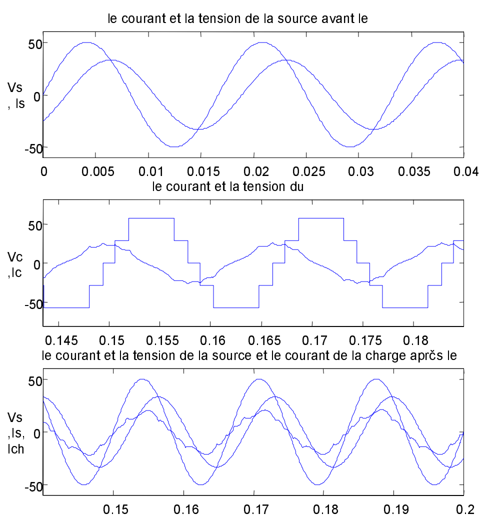

Fig.8. (a) Voltage and current of the source before compensation, (b) voltage and currant of the compensator and (c) voltage of the source and current of the source and load after compensation.

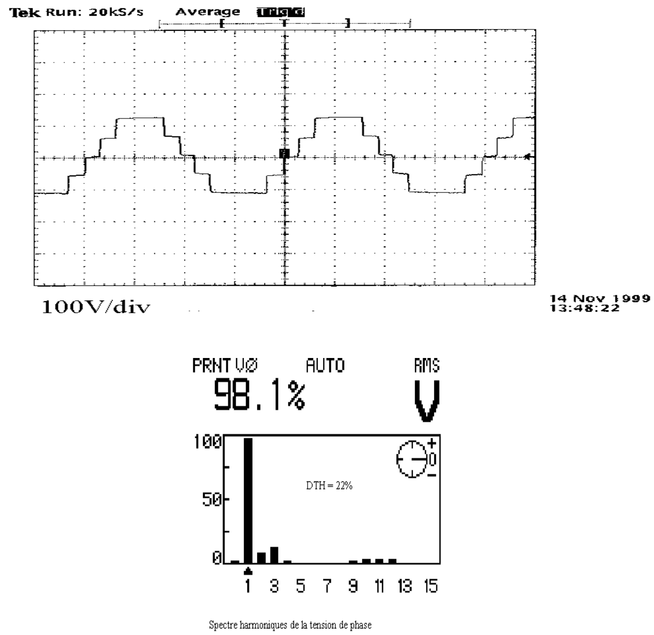

Fig.9. Output voltage waveform with its harmonic spectra

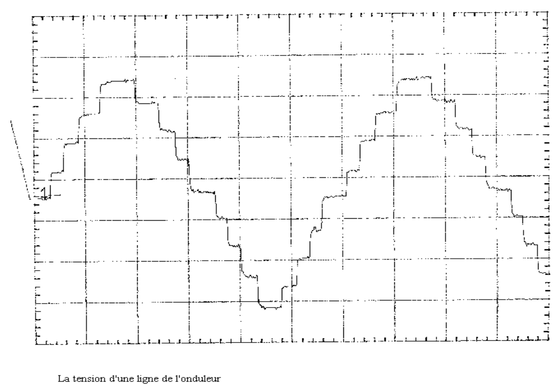

Fig.10. Nine-level line to line voltage

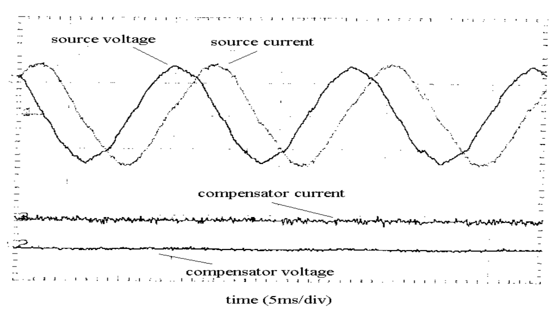

Fig.11. Voltage and current of the source and voltage and current of the compensator before compensation

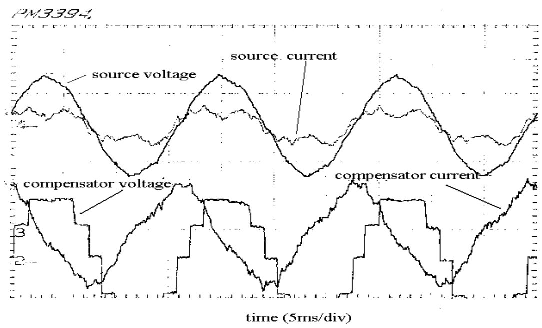

Fig.12. Voltage and current of the source and voltage and current of the compensator after compensation

VI. CONCLUSION

The diode clamped, multilevel VSI used with FFM switching strategy is very attractive configuration for high voltage application, especially as STATCOM. The FFM switching strategy minimizes switching losses and permits off line optimization what leads to decrease of harmonic content in output voltage waveform. However, during unbalanced condition, a STATCOM based on diode clamped, multilevel VSI and FFM switching strategy with off line optimization is not able to respond properly. In this case, each phase has to respond individually, with its own voltage. If the switching angles are off line chosen and fixed, than the charging or discharging of the capacitors on the DC side of inverter will affect equally all three phase. To respond properly, the PWM switching strategy should be used during unbalanced conditions or switching angles should be on line chosen. As a consequence, quantity of harmonics will increase. The second solution would be to use separate DC buses with large capacitors for each phase of inverter.

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VIII. BIOGRAPHIES

Slaven Kincic was born at Sarajevo (Bosnia). He received his B.E. degree from FER (Faculty of Electrical Engineering and Computing), Zagreb, Croatia in 1996 and M.E. degree from École de technologie supérieure, Montreal, Canada in 2000. Currently he is working toward Ph.D. degree at ETS, University of Quebec, Montreal, Canada. His main research interests are FACTS, Power Electronics, Power Systems, Electrical Machines and Drives.

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